1. (Currently Amended) A method of operating a processor to repeatedly execute an [[associated]] instruction, comprising:

loading a register with a count value indicative of the number of times [[the associated]] a single instruction is to be executed;

fetching and executing a REPEAT instruction indicating the [[associated]] single instruction to be repeatedly executed;

fetching the [[associated]] single instruction; and

repeatedly executing the [[associated]] single instruction for as many times as indicated by the count value without refetching the [[associated]] single instruction .

2. (Currently Amended) A method of operating a processor to repeatedly execute an instruction comprising:

fetching a REPEAT instruction;

executing a REPEAT instruction, wherein execution of the REPEAT instruction stores in a register a count value indicative of the number of times [[an associated]] a single instruction is to be executed;

fetching the [[associated]] single instruction; and

repeatedly executing the associated instruction for as many times as indicated by the count value.

3. (Currently Amended) A method of operating a processor to repeatedly execute an instruction comprising:

loading a register with a count value indicative of the number of times [[an associated]] a single instruction is to be executed;

fetching and executing a REPEAT instruction indicating the [[associated]] single instruction that is to be repeatedly executed;

incrementing a program counter;

fetching the [[associated]] single instruction; and

repeatedly executing the [[associated]] single instruction for as many times as indicated by a count value stored in a count register.

4. (Original) A method of operating a processor according to claim 3, wherein said count value is stored in said count register before execution of said REPEAT instruction.

5. (Original) A method of operating a processor according to claim 3, wherein said REPEAT instruction includes the count value that is stored in said count register, wherein execution of the REPEAT instruction stores the count value in said count register.

6. (Currently Amended) A method of operating a processor according to claim 3, wherein said method further comprises:

incrementing the program counter after the [[associated]] single instruction has been executed for as many times as indicated by the count value.

7. (Currently Amended) A method according to claim 3, wherein method further comprises:

decrementing said count value stored in said register each time said [[associated]] single instruction is executed; and

determining whether said count value is less than or equal to zero.

8. (Currently Amended) A processor for repeatedly [[execute an associated]] executing a single instruction, said processor comprising:

load means for loading a register with a count value indicative of the number of times the [[associated]] single instruction is to be executed;

first fetch means for a REPEAT instruction indicating the [[associated]] single instruction to be repeatedly executed;

first execute means for executing the REPEAT instruction indicating the [[associated]] single instruction to be repeatedly executed;

second fetch means for fetching the [[associated]] single instruction; and

second execute means for repeatedly executing the [[associated]] single instruction for as many times as indicated by the count value without refetching the [[associated]] single instruction.

9. (Currently Amended) A processor for repeatedly executing an instruction, comprising:

first fetch means for fetching a REPEAT instruction;

first execute means for executing a REPEAT instruction, wherein execution of the REPEAT instruction stores in a register a count value indicative of the number of times [[the]] a single instruction is to be executed;

second fetch means for fetching the [[associated]] single instruction; and

second execute means for repeatedly executing the [[associated]] single instruction for as many times as indicated by the count value.

10. (Currently Amended) A processor for repeatedly executing an instruction, comprising:

load means for loading a register with a count value indicative of the number of times [[an]] a single instruction is to be executed;

first fetch means for fetching a REPEAT instruction indicating the single instruction that is to be repeatedly executed;

first execute means for executing the REPEAT instruction indicating the [[associated]] single instruction that is to be repeatedly executed;

means for incrementing a program counter;

second fetch means for fetching the [[associated]] single instruction; and

second execute means for repeatedly executing the [[associated]] single instruction for as many times as indicated by a count value stored in a count register.

11. (Original) A processor according to claim 10, wherein said count value is stored in said count register before execution of said REPEAT instruction.

12. (Original) A processor according to claim 10, wherein said REPEAT instruction includes the count value that is stored in said count register, wherein execution of the REPEAT instruction stores the count value in said count register.

13. (Currently Amended) A processor according to claim 10, wherein said processor further comprises:

means for incrementing the program counter after the [[associated]] single instruction has been executed for as many times as indicated by the count value.

14. (Currently Amended) A processor according to claim 10, wherein processor further comprises:

means for decrementing said count value stored in said register each time the single instruction is executed; and

means for determining whether said count value is less than or equal to zero.

15. (Currently Amended) A processor for repeatedly executing one or more processor instructions, said processor comprising:

a memory address register associated with a main memory;

a memory data register associated with the main memory;

a memory control for generating memory control signals;

a program counter for storing a memory address location of the main memory where an instruction is to be fetched;

an instruction register for storing an instruction that is to be executed;

at least one general purpose register;

decode and execute control logic for decoding and executing an instruction stored in the instruction register; and

a state machine for controlling the fetching and repeated execution of [[an associated]] a single instruction.

16. (Currently Amended) A processor according to claim 15, wherein said processor further comprises an instruction buffer for storing the [[associated]] single instruction.

17. (Currently Amended) A processor according to claim 15, wherein said general purpose register includes a first register for storing a count value indicative of the number of times the [[one or more associated instructions are]] single instruction is to be repeatedly executed.

18. (Original) A processor according to claim 17, wherein said state machine generates signals for decrementing the count value stored in the first register.

19. (Original) A processor according to claim 17, wherein said state machine generates a signal for executing an instruction stored in said instruction register.

20. (Currently Amended) A processor according to claim 17, wherein said state machine generate a signal for incrementing said program counter after the [[associated]] single instruction is repeatedly executed.